The art of record does not show the recitations of Applicants' claims. FIG. 1 of U.S. Patent No. 6, 127, 261 to Ngo (Issued: 03 Oct. 2000; Filed: 16 November 1995) is instructive, and is reproduced as follows:

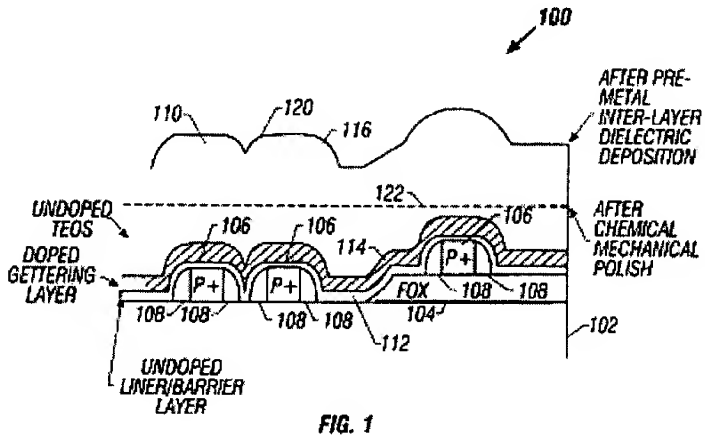


FIG. 1

With respect to FIG. 1, the text of Ngo states as follows:

> Referring to FIG. 1, a cross-sectional view of an integrated circuit 100 shows an example of a trilayer premetal interlayer dielectric deposition. The integrated circuit 100 includes a silicon substrate 102. A field oxide region 104 is formed on one side of the substrate 102 and is used to isolate devices within the substrate 102. A plurality of polysilicon gates 106 are formed overlying the substrate 102. The polysilicon gates 106 have oxide spacers 108 for implantation of structures such as lightly-doped drain (LDD) structures. A tri-layer premetal dielectric 110 overlies the surface of the substrate 102. The three layers of the tri-layer premetal dielectric 110 include an undoped liner/barrier layer 112, a doped gettering layer 114 and an undoped TEOS layer 116. A solid line 120 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after deposition of the tri-layer but before any etching or polishing. **A dotted line 122 shows the surface of the integrated circuit 100 overlying the tri-layer premetal dielectric 110 after chemical mechanical polishing.**

Ngo Patent, col. 2, lines 31-49.

> The undoped TEOS layer 116 is utilized to fill any voids in the surface of the doped gettering layer 114. **The undoped TEOS layer 116** fills voids caused by structures such as the polysilicon gates 106 and the field oxide region 104. The undoped TEOS layer 116 **also adds thickness to the surface of the integrated circuit so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered]**. The undoped TEOS layer 116 has a thickness of approximately 10200 angstroms. The total thickness of the trilayer premetal dielectric 110 is approximately 13700 angstroms with a standard deviation of approximately 200 angstroms and a final thickness after polishing of about 4000 angstroms.

Ngo Patent, col. 2, lines 65-68 and col. 3, lines 1-10 (the sentence stated above is missing the verb and applicants have placed the words "are covered" at the end because it is believed this is what was intended by the inventor and corresponds to what is shown in the figure).

As noted, Ngo teaches that its "**undoped TEOS layer 116 ... adds thickness to the surface of the integrated circuit so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered].**" From the specification teachings regarding the structure of Ngo, looking at Figure 1 of Ngo two teachings of Ngo are clear. First, Ngo stops the etch of the TEOS layer 116 well before exposing the upper gettering layer 114. Namely, the dotted line 122 in Figure 1 is well above the upper surface of the doped gettering layer 114 such that the doped gettering layer is not exposed. Second, Ngo teaches that the thickness of the overall structure is increased. Ngo specifically states that the layer 116 is made sufficiently thick that even after the polishing, it is sufficiently thick that all prominent structures including the regions over the field oxides and the polysilicon are completely covered. This second teaching also indicates that it is desired to add to the thickness of the structure as a whole.

Figure 7b of U.S. Patent No. 5,503,882 to Dawson is instructive and is reproduced as follows:

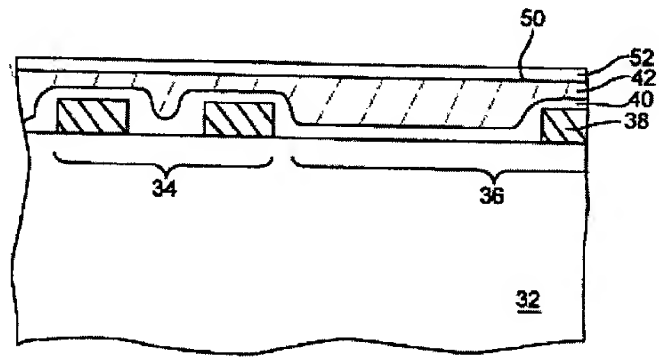


Fig. 7b

With respect to FIG. 7b, the text of Dawson states as follows:

> Alternatively, capping layer 52 can be placed upon an etch-back upper surface 50 of FIG. 6b, as shown in FIG. 7b. Capping layer 52, in either embodiments of FIG. 7a or 7b, provide the advantages described above. Capping layer 52 upon etch-back upper surface 50, shown in FIG. 7b, ensures that the lower density TEOS oxide will not absorb moisture from an outside ambient. Capping layer 52 provides a barrier against absorption similar to the barrier formed above SOG layer 46, as shown in FIG. 7a.

Dawson Patent, col. 9 lines 20-30

Applicants have herein amended claim 1 to recite to recite "a planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a first portion of the layer of the borophosphorous silicate glass, and not overlaying at least a second portion of the borophosphorous silicate glass layer, the second portion separated by a distance from the first portion; and a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least the second portion of the borophosphorous silicate glass region, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and said layer of plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack...." As can be seen from Ngo's Fig. 1 and supporting text, Ngo does not show the foregoing recitations of claim 1.

Dawson does not teach modifying the structures of Ngo to reach the recitations of Applicants' claim 1. The Examiner has stated that Dawson, in Figure 7B, is related art because in the Examiner's view it teaches a planarized layer of PETEOS 42 being overlaid by a capping layer of PETEOS 52. *Examiner's Office Action* (03 Oct. 2002). Applicants point out that even if there were a teaching to modify Ngo with the teachings of Dawson (which Applicants contest, below), this teaching of Dawson would not provide the missing teachings of Ngo. As can be seen in Fig. 7b of Dawson, the layer 42 is not etched sufficiently to expose the layer below it, layer 40, rather the layer 42 provides a single upper surface. More specifically, the Examiner was of the view that it would be obvious from the combination of Dawson and Ngo to extend the capping layer in contact with the BPSG layer. Applicants strongly disagree. The clear teaching of Dawson is that the layer 52 resides on top of another PETEOS layer 42 and does not contact nor directly overlay and contact with any lower surface portions. Dawson reinforces the shortcomings of Ngo. Namely, both Dawson and Ngo clearly teach that an upper PETEOS layer is to be provided which adds to the overall thickness of the structure. There is no suggestion or teaching in either of the references that the capping layer is to be in contact with a BPSG layer or some lower layer. Instead, the teaching is directly the opposite, namely, that the capping layer must not be in contact with a BPSG layer or any layer below. Accordingly, even if Ngo and Dawson were combined, they would still fail to teach the "planarized layer of plasma-enhanced

tetraethyl orthosilicate over at least a first portion of the layer of the borophosphorous silicate glass, and not overlaying at least a second portion of the borophosphorous silicate glass layer, the second portion separated by a distance from the first portion; and a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least the second portion of the borophosphorous silicate glass region, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and said layer of plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack...."recitations of claim 1.

Applicants have herein amended claim 6 to recite "an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said unplanar layer having an uppermost surface; a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and a second dielectric layer disposed on the planar dielectric layer and the uppermost surface of said unplanar layer of borophosphorous silicate glass, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and said second dielectric layer together composing a pre-metal dielectric stack." As can be seen from Ngo's Fig. 1 and supporting text, Ngo does not show the foregoing recitations of herein amended claim 6. As can be seen in Fig. 7b of Dawson, layer 52 resides on top of another PETEOS layer 42. Accordingly, even if Ngo and Dawson were combined, they would still fail to teach at least the "an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said unplanar layer having an uppermost surface; a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and a second dielectric layer disposed on the planar dielectric layer and the uppermost surface of said unplanar layer of borophosphorous silicate glass, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and said second dielectric layer together composing a pre-metal dielectric stack" recitations of herein amended claim 6.

Applicants' claim 20 recites "a layer of doped silicate glass over the layer of undoped silicate glass and having a physical contour of recessed and extended portions corresponding to the physical contour of the layer of undoped silicate glass; a first substantially planar layer of dielectric material covering at least one or more of the recessed portions of the layer of the doped silicate glass, and exposing at least one or more of the extended portions of the layer of the doped silicate glass layer; and a second layer of dielectric material covering the first substantially planar layer of dielectric material and being in direct contact with the at least one or more extended portions of the layer of the doped silicate glass layer" As can be seen from Ngo's Fig. 1 and supporting text, Ngo does not show the foregoing recitations of claim 20. As can be seen in Fig. 7b of Dawson, layer 52 resides on top of another PETEOS layer 42. Accordingly, even if Ngo and Dawson were combined, they would still fail to teach at least the "a layer of doped silicate glass over the layer of undoped silicate glass and having a physical contour of recessed and extended portions corresponding to the physical contour of the layer of undoped silicate glass; a first substantially planar layer of dielectric material covering at least one or more of the recessed portions of the layer of the doped silicate glass, and exposing at least one or more of the extended portions of the layer of the doped silicate glass layer; and a second layer of dielectric material covering the first substantially planar layer of dielectric material and being in direct contact with the at least one or more extended portions of the layer of the doped silicate glass layer" recitations of claim 20.

Applicants have added new claim 28 to recite "a layer of borophosphorous silicate glass over the layer of undoped silicate glass, said layer of borophosphorous silicate glass having an upper surface having a highest surface region and a lowest surface region; a planarized layer of plasma-enhanced tetraethyl orthosilicate disposed on said layer of borophosphorous silicate glass said planarized layer having a thickness less than or approximately equal to a difference in the highest surface region and the lowest surface region of the BPSG layer; and a layer of plasma-enhanced tetraethyl orthosilicate overlaying and being in contact with the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with the highest surface region of the borophosphorous silicate glass region...." Ngo does not show the foregoing recitations of claim 28. The art of record does not teach modifying the structure of Ngo to reach Applicants' claim 28 recitations

As pointed out above, Applicants challenge that there is at teaching to combine Ngo and Dawson, and assert that there cannot be such a teaching as a matter of law. Applicants point out that Ngo teaches that its "**undoped TEOS layer 116 ... adds thickness to the surface of the integrated circuit so that all structures, even prominent structures overlying both the field oxide region 104 and the polysilicon gate 106 [are covered].**" The direct teaching of Ngo is to stop etching at line 122 of his Figure 1 so as to provide protection to even the most prominent structures. If the structure of Ngo were to be modified to reach the recitations of any of Applicants' claims 1, 6, 20, and 28 the structure of Ngo would no longer be fit to serve its stated purpose, in that **the "prominent structures overlying both the field oxide region 104 and the polysilicon gate 106" would no longer be covered.** As stated in the MPEP there can be no teaching to combine if a proposed modification would render a prior art device. *MPEP* § 2143.01 ("the proposed modification cannot render the prior art unsatisfactory for its intended purpose"). Accordingly, not only is there no teaching to combine Ngo with Dawson, there cannot be such a teaching as a matter of law. Consequently, the art of record does not render any of Applicant's pending independent claims obvious for at least the reason that no teaching to combine the references exists in the art..

All remaining claims depend either directly or indirectly from claims 1, 6, 20, or 28, and thus are not rendered unpatentable by the art of record for at least the reasons why claims 1, 6, 20, or 28 are not rendered unpatentable.

Patentability now established, the remainder of the rejections are rendered moot, and hence Applicants do not explicitly address such moot rejections herein. The fact that the moot rejections are not addressed should not be taken as an admission of any sort, and Applicants reserve the right to contest the statements in such moot rejections at a later time, should such become necessary.

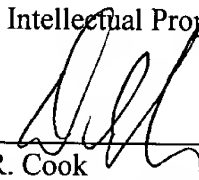
Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**Version With Markings to Show Changes Made.**" If a conflict arises between the clean copy and the attached "**Version With Markings to Show Changes Made,**" this statement constitutes public notice that Applicants respectfully request that their intent is that the version with changes made be considered controlling.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

Shin Hwa Li et al.

SEED Intellectual Property Law Group PLLC



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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Please amend claims 1 and 6 to read as follows:

1. (Thrice Amended) A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass;

a planarized layer of plasma-enhanced tetraethyl orthosilicate over at least a first portion of the layer of the borophosphorous silicate glass, and not overlaying at least a second portion of the borophosphorous silicate glass layer, the second portion separated by a distance from the first portion; and

a layer of plasma-enhanced tetraethyl orthosilicate overlaying the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with at least athe second portion of the borophosphorous silicate glass region, ~~the layers~~ said layer of ~~the~~ undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and ~~second~~ said layer of plasma-enhanced tetraethyl orthosilicate ~~layer~~ together forming a pre-metal dielectric stack.

2. The structure of claim 1 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2,000 and 8,000 angstroms.

3. The structure of claim 1 wherein the second layer of plasma-enhanced tetraethyl orthosilicate is planar.

4. The structure of claim 3 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than 15,000 angstroms.

6. (Thrice Amended) An integrated circuit, comprising:

a substrate;

a first dielectric layer disposed on the substrate;

a layer of undoped silicate glass disposed on the dielectric layer;

an unplanar layer of borophosphorous silicate glass disposed on the layer of undoped silicate glass, said planar layer having an uppermost surface;

a planar dielectric layer disposed on the unplanar layer of borophosphorous silicate glass~~, the planar dielectric layer directly overlaying at least a portion of the borophosphorous silicate glass and leaving exposed so as to not directly overlay at least a portion of the borophosphorous silicate glass~~, said planar dielectric layer having an uppermost surface substantially even with the uppermost surface of said unplanar layer of borophosphorous silicate glass; and

a second dielectric layer disposed on the planar dielectric layer and the ~~portions of the borophosphorous silicate glass which are not overlaid by the planar dielectric layer~~ uppermost surface of said unplanar layer of borophosphorous silicate glass, ~~the layers~~ said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planar dielectric layer, and ~~a~~ said second dielectric layer together composing a pre-metal dielectric stack.

7. The integrated circuit of claim 6 wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

9. The integrated circuit of claim 6 wherein the second dielectric layer is tetraethyl orthosilicate

10. The integrated circuit of claim 6 wherein the second dielectric layer is plasma-enhanced tetraethyl orthosilicate disposed on the planar dielectric layer; and

wherein the planar dielectric layer comprises plasma-enhanced tetraethyl orthosilicate.

20. A semiconductor device sub-structure, comprising:

a substrate;

an oxide layer disposed over the substrate in a pattern having a physical contour of at least one or more recessed portions and at least one or more extended portions;

a layer of undoped silicate glass disposed over the patterned oxide layer and having a physical contour of recessed and extended portions corresponding to the physical contour of the oxide layer;

a layer of doped silicate glass over the layer of undoped silicate glass and having a physical contour of recessed and extended portions corresponding to the physical contour of the layer of undoped silicate glass;

a first substantially planar layer of dielectric material covering at least one or more of the recessed portions of the layer of the doped silicate glass, and exposing at least one or more of the extended portions of the layer of the doped silicate glass layer; and

a second layer of dielectric material covering the first substantially planar layer of dielectric material and being in direct contact with the at least one or more extended portions of the layer of the doped silicate glass layer.

22. The device of claim 20 wherein the layer of doped silicate glass is a layer of borophosphorous silicate glass.

23. The device of claim 22 wherein the first layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

24. The device of claim 23 wherein the second layer of dielectric material is a layer of plasma-enhanced tetraethyl orthosilicate.

25. The device of claim 24 wherein the second layer of dielectric material is substantially planar.

26. The device of claim 25 wherein the layer of borophosphorous silicate glass has a thickness between approximately 2,000 and 8,000 angstroms.

27. The device of claim 26 wherein a combined thickness of the oxide layer, the layer of undoped silicate glass, the layer of borophosphorous silicate glass, and the second layer of plasma-enhanced tetraethyl orthosilicate is less than 15,000 angstroms.

28. (New) A semiconductor structure, comprising:

a substrate;

a patterned oxide layer disposed over the substrate;

a layer of undoped silicate glass disposed over the patterned oxide layer;

a layer of borophosphorous silicate glass over the layer of undoped silicate glass, said layer of borophosphorous silicate glass having an upper surface having a highest surface region and a lowest surface region;

a planarized layer of plasma-enhanced tetraethyl orthosilicate disposed on said layer of borophosphorous silicate glass said planarized layer having a thickness less than or approximately equal to a difference in the highest surface region and the lowest surface region of the BPSG layer; and

a layer of plasma-enhanced tetraethyl orthosilicate overlaying and being in contact with the planarized layer of plasma-enhanced tetraethyl orthosilicate and directly overlaying and being in contact with the highest surface region of the borophosphorous silicate glass region, said layer of undoped silicate glass, said layer of borophosphorous silicate glass, said planarized plasma-enhanced tetraethyl orthosilicate, and said layer of plasma-enhanced tetraethyl orthosilicate together forming a pre-metal dielectric stack.